**Group-5 Bug-4**

1. **Failing Test name**

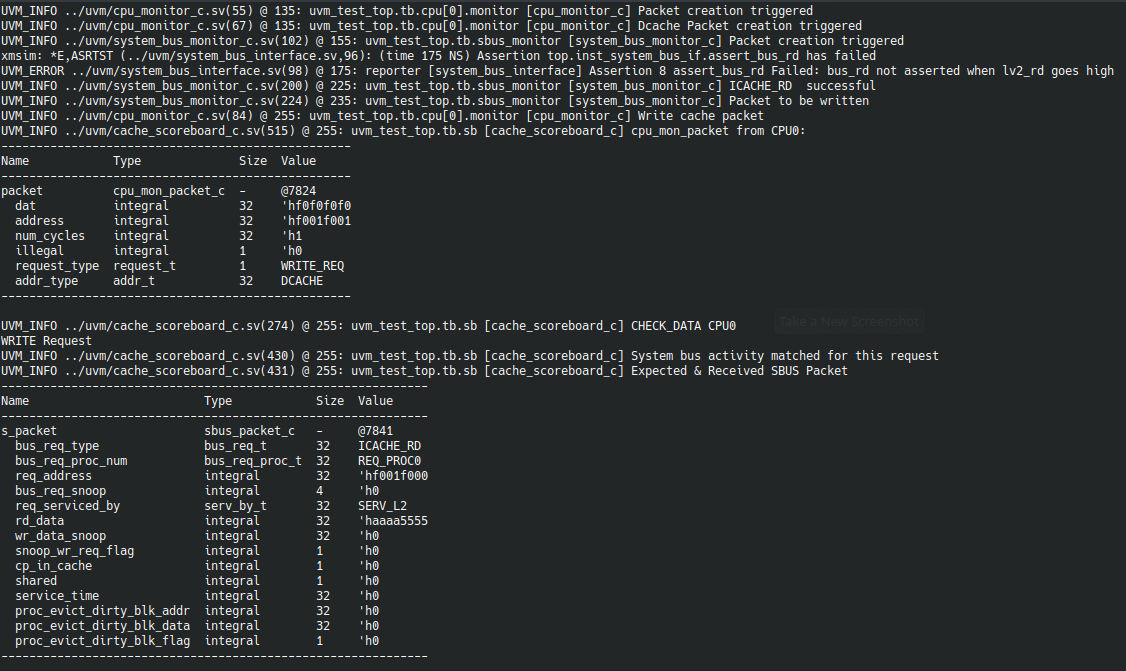
Data cache Write Miss Test

1. **Test description (Describe the planned scenario and the expected result)**

write\_miss\_dcache: A basic write on the data cache was executed, resulting in a miss, and was expected to get data from level-2 cache. This was done on all CPUs to ensure full coverage.

1. **Failing assertion that helped you identify the bug**

Error message:



1. **Debug Process**

It was found that neither bus\_rd nor bus\_rdx was being asserted on a lv2\_rd. Since this is a write test and since read tests had satisfied this assertion previously, we expect bus\_rdx to be asserted in this case.

To check why, the design file was searched for assignment to bus\_rdx, and an error was found.

1. **Erroneous RTL file name**

main\_func\_lv1\_dl.sv

1. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**

248. bus\_rdx\_reg <= 1'bz;

1. **Corrected RTL code (only mention the corrections)**

248. bus\_rdx\_reg <= 1'b1;